[0138] FIG. **17** is a block diagram illustrating a computing system including the semiconductor memory device according to exemplary embodiments.

[0139] Referring to FIG. **17**, a computing system **800** may be mounted on a mobile device or a desktop computer. The computing system **800** may include a memory system **810**, a central processing unit (CPU) **820**, a RAM **830**, a user interface **840**, and a modem **850** such as a baseband chipset, which are electrically connected to a system bus **805**. The computing system **800** may further include an application chipset, a camera image processor (CIS), and an input/output device.

[0140] The user interface **840** may be an interface for transmitting data to a communication network or receiving data from the communication network. The user interface **840** may have a wired or wireless form, and may include an antenna or a wired/wireless transceiver. Data applied through the user interface **840** or the modem **850** or processed by the CPU **820** may be stored in the memory system **810**.

[0141] The memory system **810** includes a semiconductor memory device **812** and a memory controller (MC) **811**. The semiconductor memory device **812** may be a DRAM. Data processed by the CPU **820** or external data is stored in the semiconductor memory device **812**. The memory controller **811** and the semiconductor memory device **812** may exchange an error vector in a code validation mode. The semiconductor memory device **812** may employ the semiconductor memory device **200***a* of FIG. **3**. The memory controller **811** may transmit to the semiconductor memory device **812**, an initializing write command IDW_CMD to direct the cell data initializing operation, or the power-up signal PWRUP, and the semiconductor memory device **812** may perform the cell data initializing operation in response to the initializing write command IDW_CMD or the power-up signal PWRUP as described with reference to FIGS. **1** through **11**.

[0142] When the computing system **800** is a device that performs wireless communications, the computing system **800** may be used in a communication system such as code division multiple access (CDMA), global system for mobile communication (GSM), North American multiple access (NADC), or CDMA2000. The computing system **800** may be mounted on an information processing device such as a personal digital assistant (PDA), a portable computer, a web tablet, a digital camera, a portable media player (PMP), a mobile phone, a wireless phone, or a laptop computer.

[0143] Aspects of the present inventive concept may be applied to systems using semiconductor memory devices. For example aspects of the present inventive concept may be applied to systems such as be a mobile phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a camcorder, personal computer (PC), a server computer, a workstation, a laptop computer, a digital TV, a set-top box, a portable game console, a navigation system, or other such electronic devices.

[0144] According to the above-described exemplary embodiments, the semiconductor memory device, before performing a normal memory operation on the memory cell array by a first unit, perform a cell data initializing operation by writing initializing bits in the memory cell array by a codeword unit different from the first unit. When the normal memory operation is performed, the semiconductor memory device performs write operation based on the initializing bits and a main data whose unit is smaller than the codeword unit. Therefore, overhead may be reduced while maintaining performance when the unit of error correction is different from a unit of read/write operation.

[0145] The foregoing is illustrative of exemplary embodiments and is not to be construed as limiting thereof. Although a few exemplary embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept as defined in the claims.

What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells;

an input/output (I/O) gating circuit configured to, before performing a normal memory operation on the memory cell array by a first unit, perform a cell data initializing operation by writing initializing bits in the memory cell array by a second unit different from the first unit; and

an error correction circuit configured to perform an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the second unit, based on the initializing bits.

2. The semiconductor memory device of claim **1**, wherein the first unit corresponds to a prefetching unit of the semiconductor memory device when the semiconductor memory device performs a read operation or a write operation, the second unit corresponds to a codeword unit of the semiconductor memory device, and the codeword unit is greater than the prefetching unit.

3. The semiconductor memory device of claim **1**, wherein the I/O gating circuit performs the cell data initializing operation in response to an initializing write command from an external device.

4. The semiconductor memory device of claim **1**, wherein the I/O gating circuit performs the cell data initializing operation in response to a power-up signal from an external device.

5. The semiconductor memory device of claim **1**, further comprising:

a register that stores a plurality of subsets and provides one of the subsets as the initializing bits in response to an initializing start signal; and

a control logic circuit configured to output the initializing start signal to the register in response to one of an initializing write command from an external device and a power-up signal from the external device.

6. The semiconductor memory device of claim **5**, wherein the initializing bits have one of a first logic level and a second logic level different from the first logic level.

7. The semiconductor memory device of claim **5**, wherein the control logic circuit is configured to generate a first control signal to control the I/O gating circuit and a second control signal to control the error correction circuit in response to one of the initializing write command and the power-up signal.

8. The semiconductor memory device of claim **5**, wherein when the semiconductor memory device performs a write